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(54) Delay control in a digital radio transmitter system

(57) A device (200) for controlling a relative delay between analog R.F. output signals of a plurality of digital radio transmitters (102, 104) in a digital radio transmitter system (100) is described. The device (200) comprises at least one interface (206a, 206b) for receiving delay information, a processing unit (206) for determining the relative delay between the output signals based on the received delay information and an adjusting system for adjusting in the digital domain the absolute delay of at least one of the radio transmitters (102, 104) in accordance with the determined relative delay. The invention further relates to a method for controlling a relative delay between analog R.F. output signals of a plurality of digital radio transmitters (102, 104).

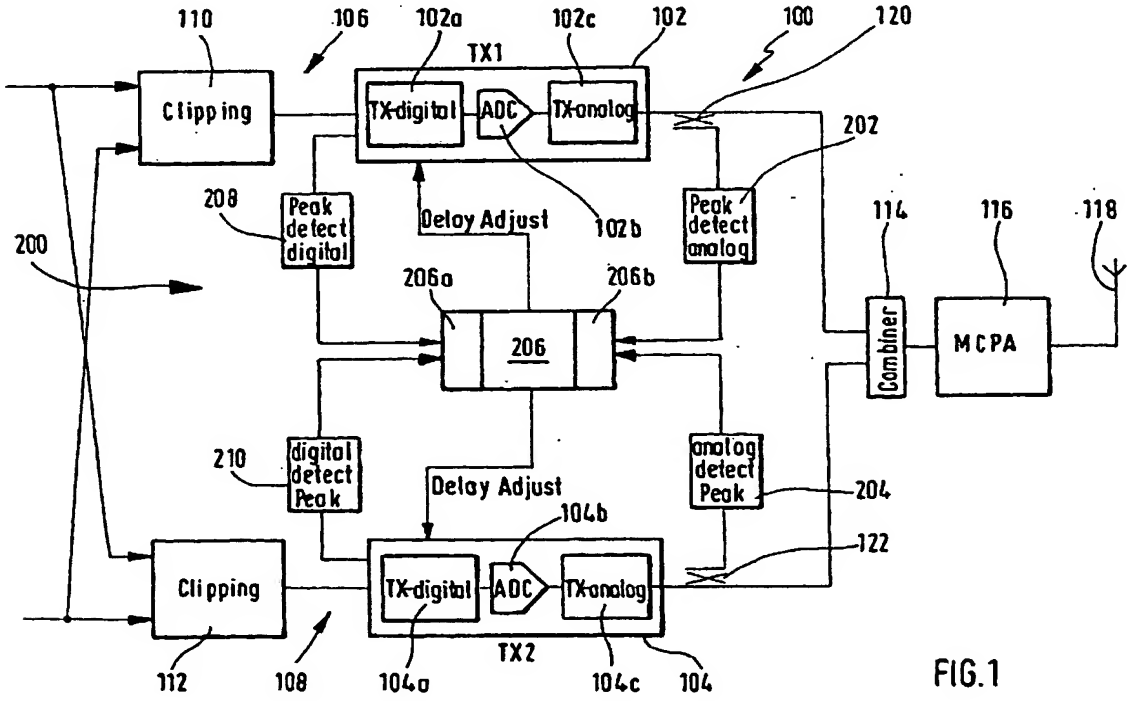

FIG.1

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tween analog R.F. output signals of a plurality of digital radio transmitters in a digital radio transmitter system, the device comprising at least one interface for receiving delay information, a processing unit for determining the relative delay between the output signals based on the received delay information, and an adjusting system for adjusting in the digital domain the absolute delay of at least one of the radio transmitters in accordance with the determined relative delay.

[0012] According to the invention, the relative delay between the analog R.F. output signals of a plurality of digital radio transmitters is controlled by receiving delay information, by determining the relative delay between the output signals based on the received delay information, and by adjusting in the digital domain the absolute delay of at least one of the radio transmitters in accordance with the determined relative delay.

[0013] Until now, delays of radio transmitters are generally determined during production of the radio transmitters and for individual transmitters only. The invention, however, enables the determination of the relative delay during operation of the radio transmitter system and preferably during regular operation, i.e., while the radio transmitter system transmits user data. Thus, the relative delay can be monitored and, if necessary, be adjusted continuously or in specified time intervals while the radio transmitter system is in an active state. This ensures a constantly high transmission quality of the radio transmitter system. Moreover, since the relative delay is controlled by adjusting the absolute delay of one or more radio transmitters in the digital domain, i.e., prior to a digital-analog conversion step in the radio transmitter, the absolute delay and thus the relative delay can be accurately adjusted. This is due to the fact that the adjustment is advantageously performed digitally and not by means of analog components subject to significant delay tolerances. Also, adjustment in the digital domain ensures that the radio transmitter characteristics are not compromised by additional analog components in the analog part of the radio transmitter.

[0014] The adjustment of a radio transmitter's absolute delay can be performed with various objects in respect to the absolute delay between two or more output signals. Preferably, the absolute delay of one or more radio transmitters is adjusted such that the relative delay is minimized. However, certain applications may require the adjustment of the absolute delay such that the relative delay of the output signals assumes a specific value which need not necessarily be the minimal value.

[0015] The one or more interfaces for receiving delay information can be configured in various ways. For example, the interfaces can be realized as hardware solution or software solution depending on the nature of the delay information to be received.

[0016] According to one embodiment of the invention, the interface receives delay information from the individual radio transmitters. Each radio transmitter may comprise a delay database in which the measured delay of the individual transmitter is stored. The measuring and storing of the delay can be performed e.g. during production of the radio transmitter board. The processing unit may receive the individual delay of each radio transmitter via the interface and may then determine the relative delay between the output signals of the radio transmitters based on the received delay information.

[0017] According to a further embodiment, the control device according to the invention further comprises a detector system for detecting the analog R.F. output signals of the radio transmitters. The detected output signals are transmitted as delay information to the processing unit via the interface. The processing unit may then determine the relative delay between the output signals detected by the detector system.

[0018] The detector system for detecting the analog R.F. output signals of the radio transmitters can be configured to detect the output signals prior to their emission from an antenna system or after they have been emitted from an antenna system. According to a first embodiment, the detector system comprises a plurality of analog detector units and each detector unit is arranged such that it detects an analog output signal of one of the radio transmitters before an antenna to which this radio transmitter is connected. According to a second embodiment, the detector system comprises one or more detection antennas for detecting the analog R.F. output signals after they have been emitted by an antenna system of the digital radio transmitter system.

[0019] Depending on the arrangement of the plurality of digital radio transmitters in the digital radio transmitter system, the antenna system of the digital radio transmitter system may have different configurations. According to one embodiment, the two or more output signals of the two or more radio transmitters are combined by a combining unit and the combined signal is fed to an antenna system in the form of a single antenna. In such a case, the output signals of the radio transmitters are preferably detected prior to their combining. A single antenna for a plurality of radio transmitter branches is e.g. employed for operating a digital radio transmitter system in a multi-carrier mode. According to a further embodiment, each radio transmitter is connected to an individual antenna. Thus, the number of antennas of the antenna system may equal the number of radio transmitters. Separate antennas for separate radio transmitters are e.g. employed for operating a digital radio transmitter system in a radio transmitter diversity mode, in a load-sharing mode or in a redundancy mode. The two embodiments illustrated above can be combined such that a plurality of combining units is provided, each combining unit being coupled to a plurality of radio transmitters which then feed the combined output signals to a single antenna.

[0020] The output signals of the radio transmitters can be detected in many ways depending on the nature of the output signals. As an example, the output signals may be detected in the form of specific signal structures

Fig. 8 shows a more detailed block diagram of the adjusting system depicted in Fig. 5.

DESCRIPTION OF PREFERRED EMBODIMENTS

[0028] Referring now to the accompanying drawings, the preferred embodiments of this invention are described.

[0029] In Fig. 1, schematic diagrams of a digital radio transmitter system 100 and of a device 200 for controlling a relative delay between analog R.F. output signals of two digital radio transmitters 102, 104 are illustrated. The digital radio transmitter system 100 is part of a W-CDMA base transceiver station of a cellular communication system.

[0030] The digital radio transmitter system 100 of Fig. 1 is operated in a 2-carrier mode. A first carrier is transmitted on a first radio transmitter branch 106 and a second carrier is transmitted on a second radio transmitter branch 108 of the radio transmitter system 100. Each radio transmitter branch 106, 108 comprises a clipping unit 110, 112 as well as one radio transmitter 102, 104. A first carrier transmitted on the first radio transmitter path 106 is inputted in the form of a digital baseband IQ-signal into the first clipping unit 110 and a second carrier transmitted on the second radio transmitter path 106 is inputted in the form of a digital baseband IQ-signal into the second clipping unit 112. Concurrently, information relating to the second carrier is inputted into the first clipping unit 110 and information relating to the first carrier is inputted into the second clipping unit 112. In the clipping units 110, 112 the digital signals are clipped using information of all carriers.

[0031] After clipping the first carrier and the second carrier, the clipped first carrier is inputted as a digital input signal into the first radio transmitter 102 and the clipped second carrier is inputted as a second input signal into the second radio transmitter 104. The radio transmitters 102, 104 then perform digital sampling in digital radio transmitter parts 102a, 104a, digital-analog conversion by digital-analog converters 102b, 104b, modulation and up-conversion of the received input signals in order to generate an analog R.F. output signal. The analog R.F. output signal of the first radio transmitter 102 and the analog R.F. output signal of the second radio transmitter 104 are combined by a combining unit 114, amplified by a multi-carrier power amplifier (MCPA) 116 and emitted from a single system antenna 118.

[0032] Both the first radio transmitter 102 and the second radio transmitter 104 exhibit a specific absolute delay. Due to the delay tolerances of the analog parts 102c, 104c of the radio transmitters 102, 104, the absolute delays of the two radio transmitters 102, 104 will generally not be identical. Consequently, synchronism between a digital signal travelling on the first radio transmitter branch 106 and a digital signal travelling on the second radio transmitter branch 108 will generally be lost after the behind radio transmitters 102, 104, i.e., in the analog domain. Thus, a relative delay between the output signal of the first radio transmitter 102 and the output signal of the second radio transmitter 104 will arise here. This relative delay, however, may destroy the clipping effect and thus compromise the transmission quality of the digital radio transmitter system 100.

[0033] In order to ensure a high transmission quality, the digital radio transmitter system 100 of Fig. 1 comprises a device 200 for controlling the relative delay between the analog R.F. output signals of the two digital radio transmitters 102, 104. The device 200 comprises a detector system with two analog detector units 202, 204 for detecting the analog output signals of the radio transmitters 102, 104, a processing unit 206 for determining the relative delay between the detected output signals, and an adjusting system (Figs. 6 and 7) arranged within the digital parts 102a, 104a of the radio transmitter 102, 104. The device 200 further comprises two digital detector units 208, 210 for detecting digital input signals of the transmitter units 102, 104.

[0034] The device 200 has two interfaces 206a, 206b for receiving delay information. The first interface 206a is arranged between the digital detector units 208, 210 and the processing unit 206. The first interface 206a receives delay information in the form of detector signals from the digital detector units 208, 210 and transfers these detector signals to the processing unit 206. The second interface 206b is arranged between the two analog detector units 202, 204 and the processing 206. The second interface 206b receives delay information in the form of detector signals from the analog detector units 202, 204 and transfers these detector signals to the processing unit 206.

[0035] Next, control of the relative delay between the analog output signals of the radio transmitters 102, 104 by means of the control device 200 is described.

[0036] In a first step, the absolute delay between input of a digital signal into each radio transmitter and output of a corresponding output signal is determined for each of the two radio transmitters 102, 104. In a second step, the relative delay between the output signals of the two radio transmitters 102, 104 are calculated based on the determined absolute delays. Finally, in a third step, the absolute delay of one or both of the radio transmitters 102, 104 is adjusted such that the relative delay between the output signals is minimized.

[0037] The absolute delay for the radio transmitters 102, 104 is determined as follows. Each wideband CDMA signal transmitted on radio transmitter branches 106, 108 is a statistical signal with characteristic peaks. Such a characteristic peak first appears in the digital domain of the signal and after the radio transmitter's absolute delay in the analog domain at the radio transmitter output. Thus, the time interval between appearance of the characteristic peak in the digital domain and appearance of the same characteristic peak in the analog domain of the same radio transmitter branch reflects the radio transmitter's absolute delay.

er, the digital input signal is detected by the digital detector unit 208, 210 at the input port of the radio transmitters 102, 104, i.e., prior to root raised cosine filtering.

[0049] The analog detector units 202, 204 and the digital detector units 208, 210 depicted in Figs. 1 and 2 need not necessarily be configured as peak detectors. The detector units 202, 204, 208, 210 can also be configured to detect a pre-defined signal component or symbol sequence. Detecting symbol sequences in the output signals of the radio transmitters 102, 104 makes it necessary to perform down-conversion, sampling, analog-digital conversion, demodulation and digital filtering in the analog detector units 202, 204 or in the processing unit 206 in order to obtain the symbol sequences comprised within the output signals.

[0050] In Fig. 3, a schematic diagram of a third embodiment of a device 200 for controlling the relative delay between analog R.F. output signals of two digital radio transmitters 102, 104 in a digital radio transmitter system 100 is depicted. Like the digital radio transmitter system of Fig. 2, the digital radio transmitter system 100 of Fig. 3 is operated in a radio transmitter diversity mode based on a single carrier.

[0051] In contrast to the control devices depicted in Figs. 1 and 2, the control device 200 of Fig. 3 does not comprise two interfaces but only a single interface 206a. The interface 206a is arranged between an individual delay database of each of the radio transmitters 102, 104 and the processing unit 206. The interface 206a is configured to read out the delay information stored in the delay databases of the radio transmitters 102, 104 and to provide the received delay information to the processing unit 206. The delay information stored in the individual delay databases of the radio transmitters 102, 104 relates to the absolute delay of each individual radio transmitter 102, 104 as measured during production of the radio transmitter 102, 104. Based on the absolute delay of each individual radio transmitter 102, 104 received via the interface 206a, the processing unit 206 calculates the relative delay and controls the adjusting system (not depicted in Fig. 3) such that the relative delay between the analog R.F. output signals of the two radio transmitters 102, 104 is minimized.

[0052] In Fig. 4, a fourth embodiment of a device 200 for controlling the relative delay between the analog R. F. output signals of two digital radio transmitters 102, 104 in a digital radio transmitter system 100 is illustrated. Similar to the digital radio transmitter systems depicted in Figs. 2 and 3, the digital radio transmitter system 100 of Fig. 4 is operated in a radio transmitter diversity mode. The digital radio transmitter system 100 has two radio transmitter branches 106, 108. Each radio transmitter branch 106, 108 comprises an individual radio transmitter 102, 104 an individual power amplifier 130, 132 and an individual antenna 134, 136.

[0053] The device 200 for controlling the relative delay between the analog R.F. output signals of the two digital radio transmitters 106, 108 deviates from the control device 200 of the first and second embodiment in that the output signals are not detected in the signal path prior to the antennas 134, 136 but after the output signals have been emitted from an antenna system comprising the two antennas 134, 136. The detector system of the control device 200 is constituted by a small detector antenna 212 which detects the output signals of the two radio transmitters 102, 104 after they have been emitted from the antenna system of the digital radio transmitter system 100. The signals detected by the detector antenna 212 are received by the interface 206a and inputted into the processing unit 206.

[0054] The arrangement of the detector antenna 212 relative to the antenna system of the digital radio transmitter system 100 is depicted in Fig. 5. As can be seen from Fig. 5, the detector antenna 212 is arranged symmetrically with respect to the plurality of antennas of the digital radio transmitter system 100.

[0055] The antenna system of Fig. 5 comprises three antenna pairs, each antenna pair looking in the same direction and defining one of three diversity antenna sectors 152, 154, 156. For example, the two antennas 134, 136 of the radio transmitter system 100 depicted in Fig. 4 define the diversity antenna sector 154. An antenna signal of each antenna pair is emitted in a sector with an opening angle of 120°. This helps to minimize cross interference effects because a base station in a next cell that is in the shadow of the opening angle of one of the diversity antenna sectors 152, 154, 156 can use the same frequency as the corresponding diversity antenna sector 152, 154, 156.

[0056] In the antenna system depicted in Fig. 5, a delay adjustment as exemplarily depicted in Fig. 4 has to be provided for each pair of antennas. Consequently, two more arrangements similar to the arrangement of Fig. 4 can be employed to control the delay of the two additional antenna pairs, respectively, which define the diversity antenna sectors 152 and 156. Thus, three identical processing units 206 may be provided. Alternatively, these three processing units may be combined to a single processing unit for all six radio transmitters needed to operate the antenna system of Fig. 5. This would minimize hardware requirements.

[0057] Returning now to Fig. 4, it becomes clear that the processing unit 206 is not only connected to the detector antenna 212 but is via the interface 206a in communication with the main processor 214 and the system frame sync (SFS) 216 of the base transceiver station to which the digital radio transmitter system 100 belongs. The main processor 214 informs the processing unit 206 on which channels, belonging to the different branches of the sectors, a delay measurement has to be performed and how these channels are related to the SFS in time. The SFS thus provides timing events.

[0058] In case of radio transmitter diversity the signals of one and the same channel have different pilot sequences on each antenna, the different pilot sequences being orthogonal to each other. The control device 200

is then amplified and transmitted from an antenna.

[0068] In Fig. 7, the digital part 102a of the radio transmitter 102 with an adjusting system 400 according to the invention is shown. The digital part 104a of the other radio transmitter 104 may comprise the same or a similar adjusting system 400. The digital part of the radio transmitter thus comprises an upsampling system with a plurality of sampling stages in the form of the filters 302, 304, 306, 308.

[0069] The adjusting system is switched in the upsampling system 300 and comprises several adjusting units 402, 404, 406, 408 which are arranged before, between and after the individual sampling stages, i.e., the interpolation filters 302, 304, 306, 308. The adjusting units 402, 404, 406, 408, 410 are configured as delay elements in the form of shift register stages.

[0070] Each single adjusting unit 402, 404, 406, 408, 410 allows to delay the signal by one clock circle of the sample frequency of the corresponding sampling stage. Due to the cascade of sampling stages 302, 304, 306, 308 interpolating by a factor of two, the sample frequency doubles after each sampling stage 302, 304, 306, 308. This means that the delay times of the corresponding consecutive adjusting units 402, 404, 406, 408, 410 are halved from one adjusting unit to the next adjusting unit.

[0071] In Fig. 7, z^{-k} denotes a delay by k times the clock cycle with the frequency $f_C = f_S/2^m$. Likewise, z_1^{-1} denotes a delay by one clock cycle with frequency $2f_C = f_S/2^{m-1}$ and so on. It is clear from Fig. 7 that the lowest delay is $1/f_S$ and the highest delay is the chip period $1/f_C$ or a multiple k thereof as indicated by z^{-k}. For example, if the sampling rate at the digital-analog converter 102b is f_S = 65.536 MHz and the chip rate f_C = 4.096 Mcps, the delay can be controlled in steps of 1/16 of the chip time. Since the delay element are power of two multiples of $1/f_C$, a plurality of selectors 413, 414, 416, 418, 420 which switch in the delays can easily be controlled by the bits of a binary control word 412.

[0072] In Fig. 8, an implementation of the adjusting system 400 of Fig. 6 is shown in more detail. Each adjusting unit 402, 404 406, 408, 410 consists of a register in the form of a number of parallel flip flops. The register width corresponds to the bit resolution of the signal samples transmitted over the I-signal path and the Q-signal path. Each adjusting unit 402, 404 406, 408, 410 is clocked by the sampling frequency of the corresponding sampling stage. Thus, the adjusting system 400 allows the adjustment of the absolute delay in the radio transmitter 102 in multiples of the sampling frequency of a specific sampling unit 302, 304, 306, 308, the sampling frequencies of the consecutive sampling units 302, 304, 306, 308 differing by a factor of two.

[0073] It has been pointed out in context with Fig. 7 that the first adjusting unit 402 delays by multiples k of the chip time. Preferably, the first adjusting unit 402 is realized as a cascade of register stages with the number of registers of a consecutive register stage being twice that of the preceeding register stage. Fig. 8 exemplarily illustrates the adjusting unit 402 which is constituted by the two register stages 402a, 402b having delays of one and two chip times, respectively. The adjusting unit 402 could be extended by register stages with 4, 8, 16 etc. registers. This allows the control of an entire chain of register stages by the bits of a binary control word.

[0074] Variations of the construction of the radio transmitter 102 may necessitate different configurations of the adjusting system 400. As an example, if the IQ-modulator 301 is realized as an analog component, the last adjusting unit 410 must be placed directly behind the last sampling stage (interpolation filter) 308 and before the analog IQ-modulator 301. Also, sampling stages having higher sampling factors than two can be employed. Different sampling factors would influence the delay times. Furthermore, as shown with respect to the first adjusting unit 402 of the adjusting unit depicted in Fig. 8, the adjusting units or the register stages comprised within an adjusting unit can be switched in series or in parallel in order to allow alternative control of the delay times. For example, adjusting units having delays differing by factors of two can be switched in series or adjusting units having delays differing by single delay times can be switched in parallel.

Claims

1. A device (200) for controlling a relative delay between analog R.F. output signals of a plurality of digital radio transmitters (102, 104) in a digital radio transmitter system (100), comprising:
   - at least one interface (206a, 206b) for receiving delay information;
   - a processing unit (206, 214) for determining the relative delay between the output signals based on the received delay information; and
   - an adjusting system (400) for adjusting in the digital domain (102a, 104a) the absolute delay of at least one of the radio transmitters (102, 104) in accordance with the determined relative delay.

2. The device according to claim 1, wherein the interface (206a) is configured to read out delay information from the individual radio transmitters (102, 104).

3. The device according to claim 1, further comprising a detector system (202, 204, 212) for detecting the analog R.F. output signals of the radio transmitters (102, 104).

4. The device according to claim 3,

24. The method according to claims 14 to 23, wherein the absolute delay is adjusted such that the absolute delay increases.

25. The method according to claims 14 to 24, wherein the absolute delay is adjusted during upsampling of a digital input signal of at least one of the radio transmitters (102, 104).

26. The method according to claims 14 to 25, wherein the absolute delay is adjusted in based on specific sampling frequencies used during upsampling.

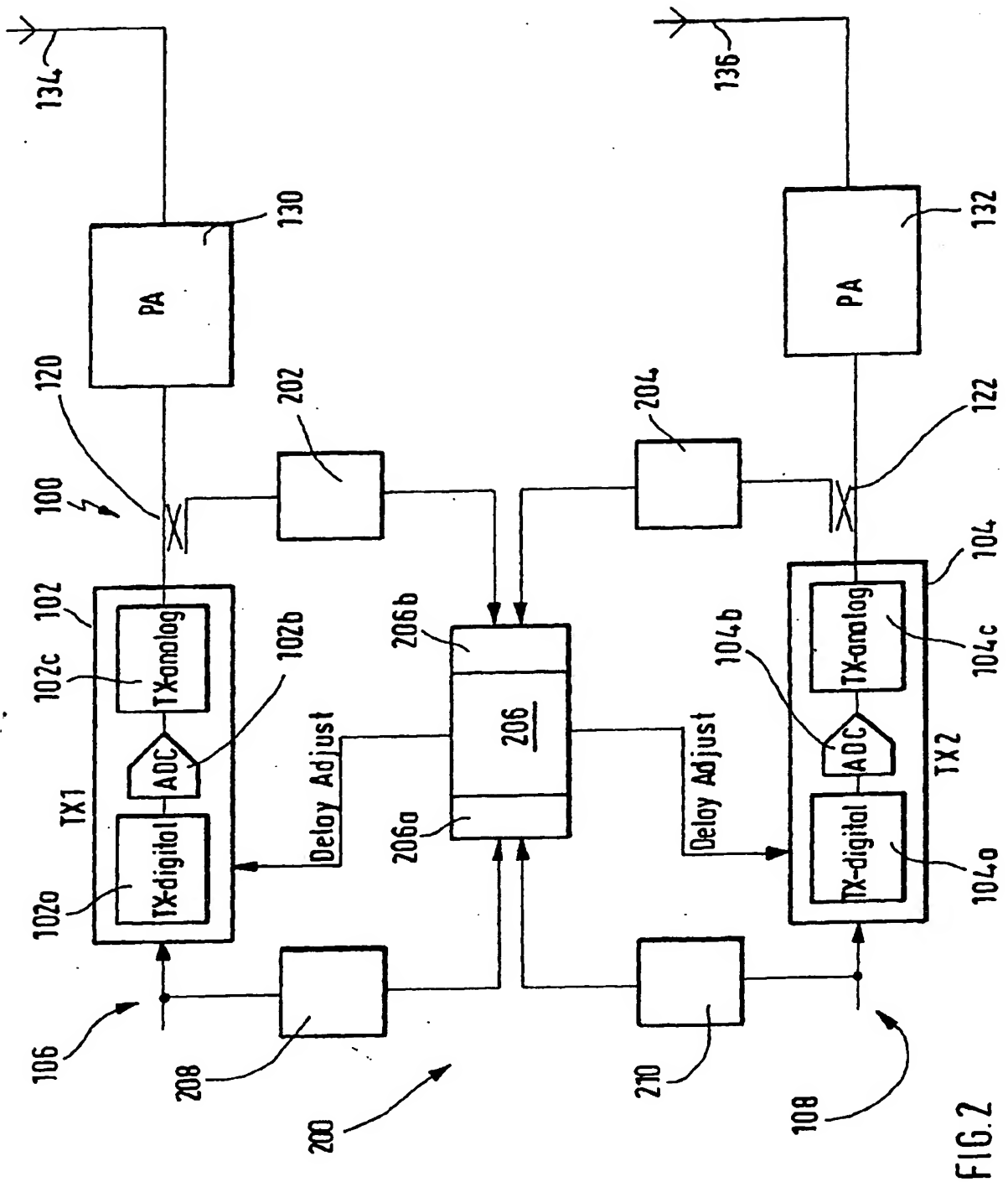


FIG.2

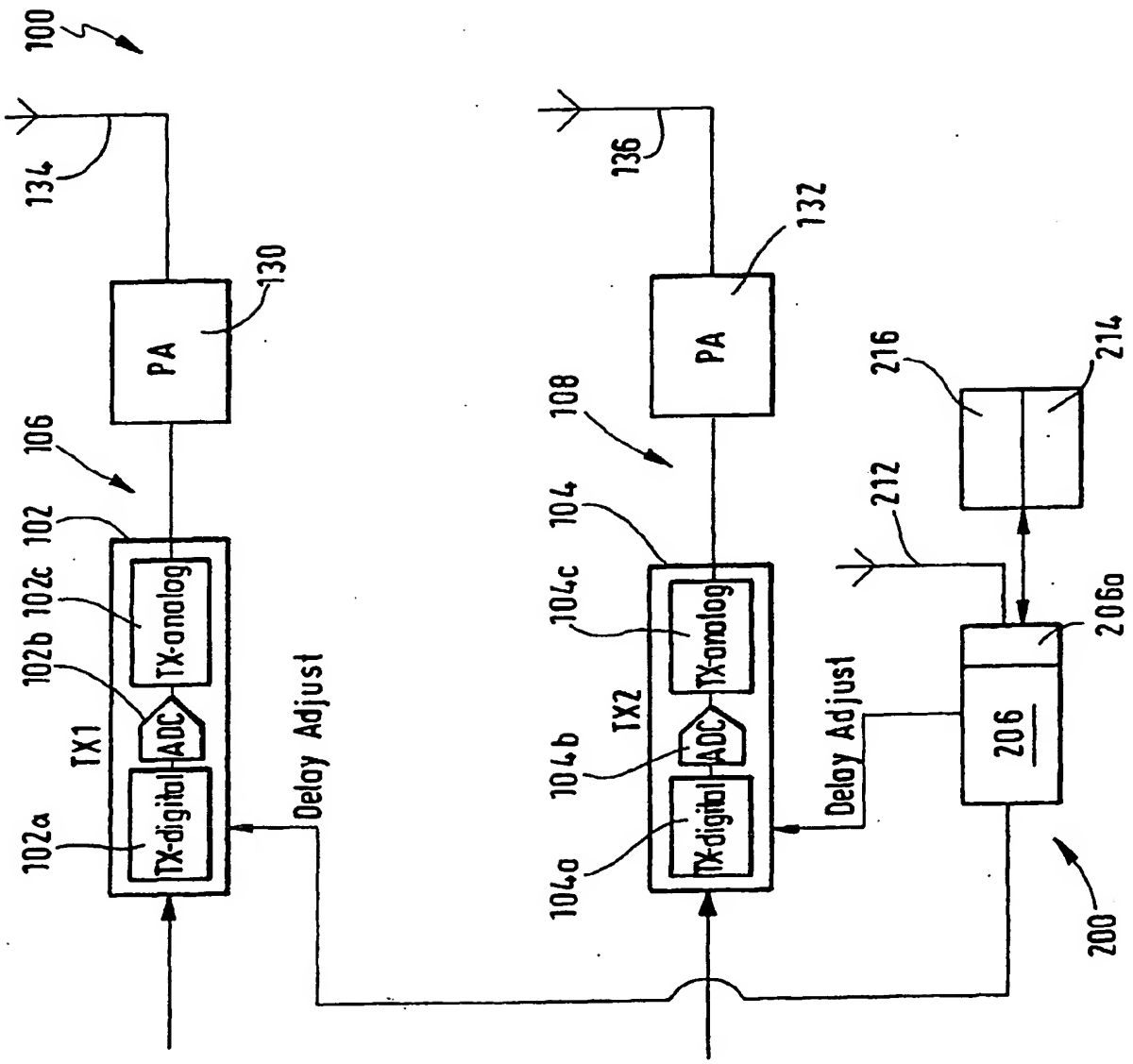
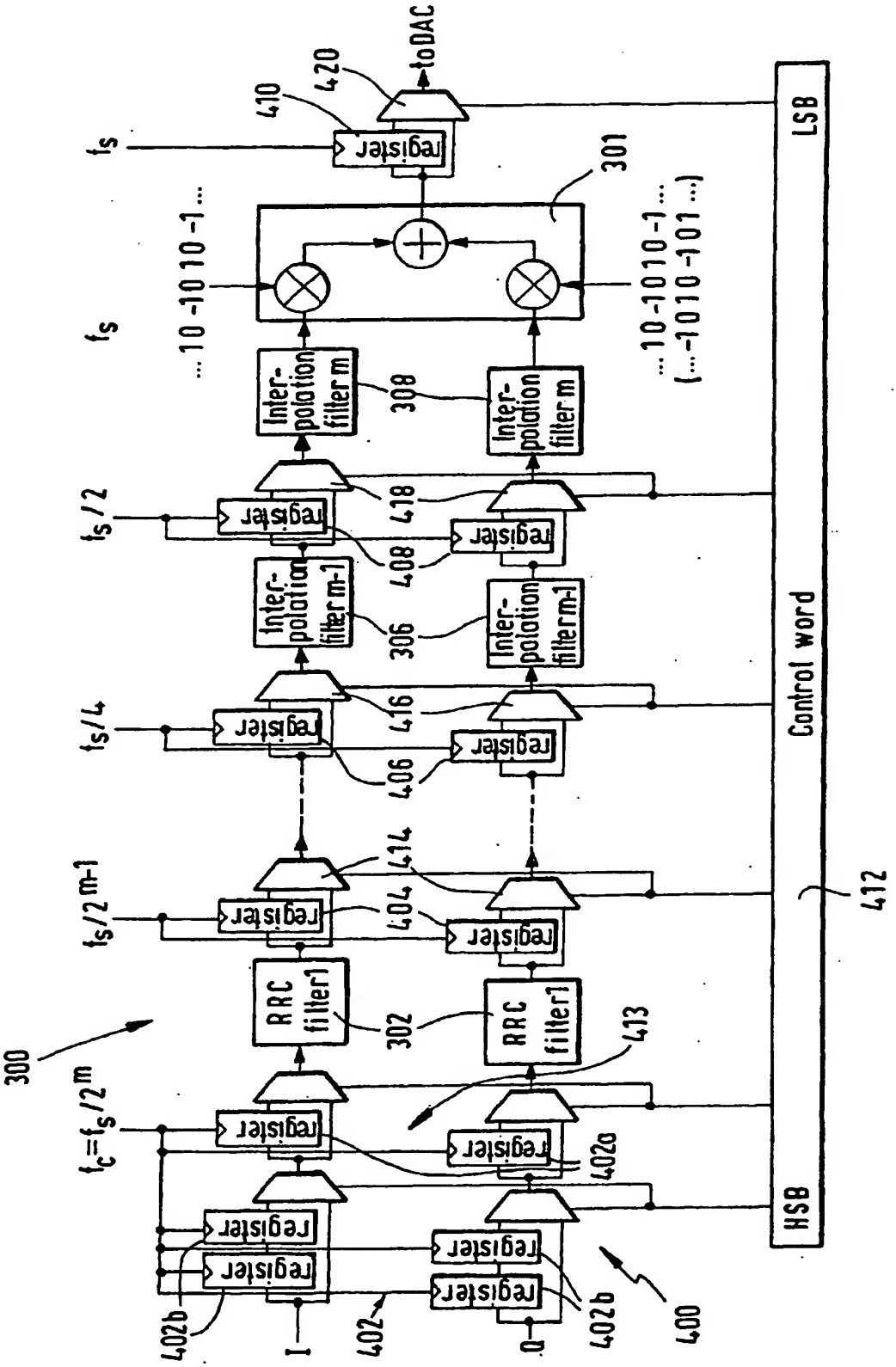


FIG. 4

FIG.6



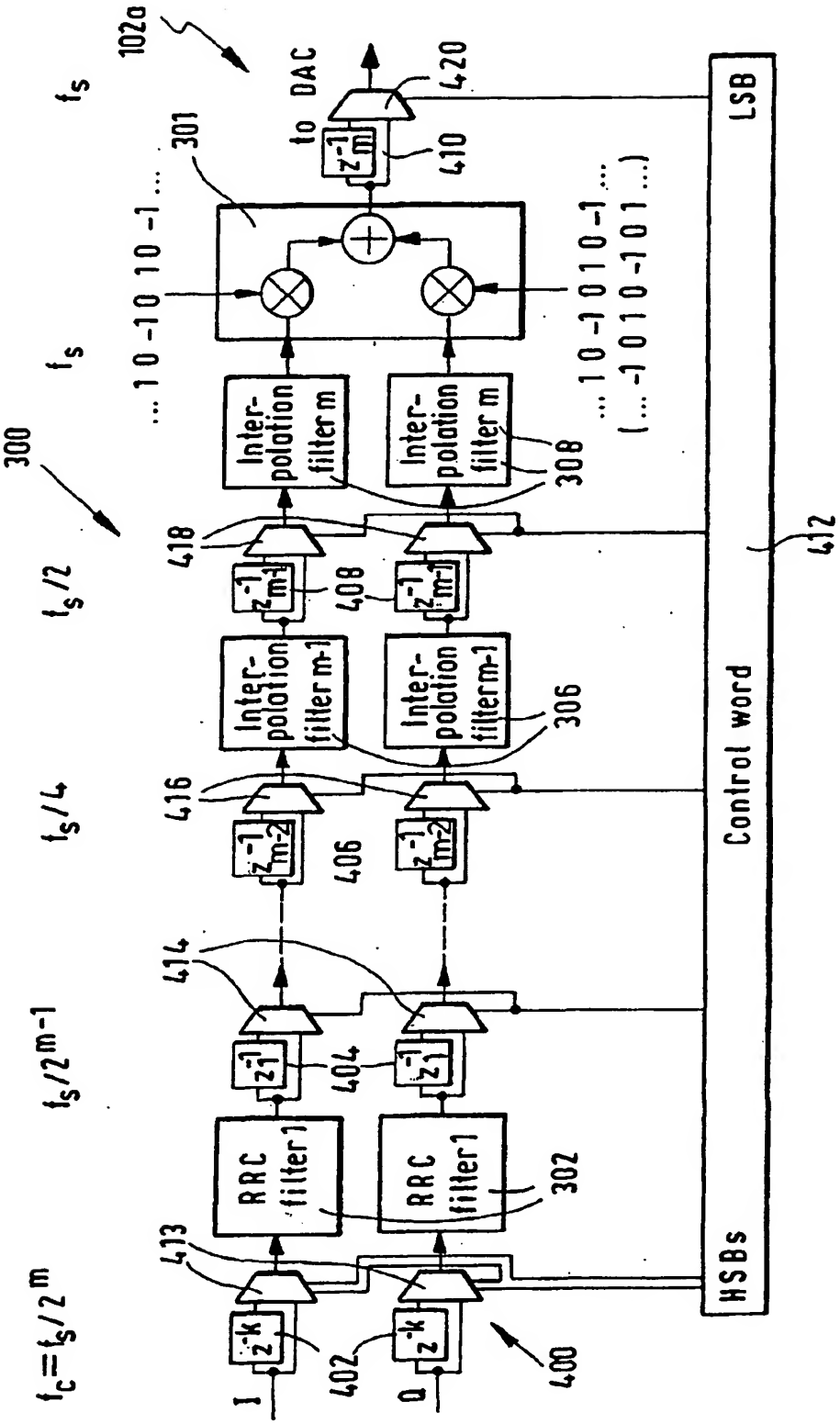


FIG.8

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 00 12 8371

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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11-01-2002

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